CBCS SCHEME

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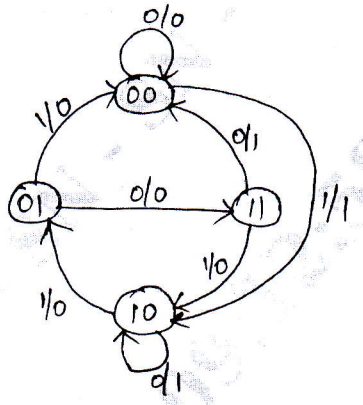
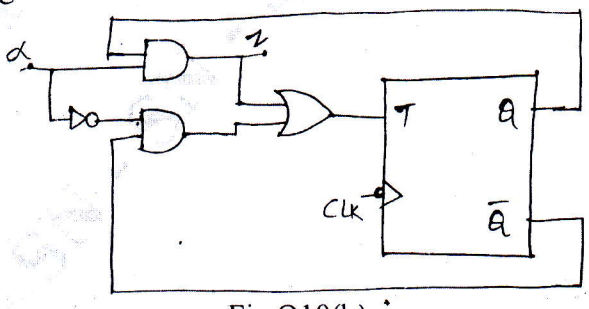
BEE306A

Third Semester B.E/B.Tech. Degree Examination, Dec.2023/Jan.2024
Digital Logic Circuits

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	Define combinational logic circuit. List the various steps in designing the combinational logic circuit and explain with a block diagram.	6	L1	CO1
	b.	Explain the canonical minterm and maxterm form with examples.	4	L1	CO1
	c.	Simplify the following Boolean function using K-map and implement using basic gates. $P = f(a, b, c, d) = \Sigma m(2, 3, 4, 5, 13, 15) + d(8, 9, 10, 11)$ $y = f(a, b, c, d) = \pi m(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$.	10	L4	CO1
		OR			
2	a.	Simplify the following expression using Quine–Mc–clusky menimisation technique. $Y = f(a, b, c, d) = \Sigma m(7, 9, 12, 13, 14, 15) + d(4, 11)$.	10	L4	CO2
	b.	Convert the following Boolean function into their proper canonical form and represent in decimal notation. i) $f = \bar{a}b + bc$ ii) $f = (\bar{x} + y)(y + \bar{z})$.	6	L4	CO2
	c.	Define the following terms : i) Literal ii) Prime implicates iii) Essential prime implicants iv) Maxterm.	4	L1	CO2
		Module – 2			
3	a.	With the aid of general structure, clearly distinguish between a decoder and an encoder.	5	L2	CO2
	b.	Design a combinational logic circuit that will convert a BCD digit to Excess-3. Construct the truth table and simplify each output equation using K-map and implement using basic gates.	10	L2	CO2
	c.	Design a 4 to 16 line decoder by cascading 2 to 4 line decoders which has the active low output and active low enable input.	5	L5	CO2
		OR			
4	a.	Design a two-bit magnitude comparator with the help of truth table and simplify the output equations using K-maps. Draw a logic diagram.	10	L5	CO2
	b.	Implement the following Boolean function using 4 : 1 MUX , $f(a, b, c) = \Sigma m(1, 3, 5, 6)$. Take b, c as select lines.	5	L5	CO2
	c.	Design a full adder by constructing the truth table and simplify the output equations.	5	L5	CO2
		Module – 3			
5	a.	Explain the operation of master-Slave JK-flip-flop with a neat logic diagram functional table, logic symbol and timing diagram.	10	L2	CO3
	b.	Explain the operation of SR Latch act as a switch debouncer with the help of timing diagram.	6	L2	CO3
	c.	Obtain the characteristic equation of JK – flip-flop and D flip-flop.	4	L4	CO3

		OR			
6	a.	Draw a neat diagram and explain the working of positive edge triggered D-flip-flop with functional table, logic symbol and timing diagram.	**10**	**L2**	**CO3**
	b.	Differentiate sequential logic circuit and combinational logic circuit.	**4**	**L2**	**CO3**
	c.	Explain the operation of gated SR latch using NAND gates.	**6**	**L2**	**CO3**
		Module – 4			
7	a.	With a neat logic diagram, explain the 4-bit universal shift register using D-flip-flops and a 4 : 1 MUX. Write a mode control and register operation.	**10**	**L2**	**CO4**
	b.	Explain the working of 4-bit binary ripple counter using a positive edge trigger T-flip-flop with an enable line and relevant timing diagram.	**10**	**L2**	**CO4**
		OR			
8	a.	Design a synchronous counter to count the sequence 0, 1, 4,6, 7, 5 and repeat using positive edge trigged JK Flip-flops.	**12**	**L5**	**CO4**
	b.	Design a 4-bit mod-8 Johnson counter and also write the count sequence table.	**8**	**L5**	**CO4**
		Module – 5			
9	a.	Explain Mealy and Moore model in a sequential circuit analysis.	**8**	**L2**	**CO5**
	b.	Design a clocked synchronous sequential network based on the state diagram given below Fig.Q9(b) using T-flip-flops.  Fig.Q9(b)	**12**	**L4**	**CO5**
		OR			
10	a.	Write short notes on : i) ROM ii) RAM iii) EPROM iv) Memory Flash.	**8**	**L4**	**CO6**
	b.	Analyse the following sequential logic circuit as shown in Fig.Q10(b) below. Obtain the excitation and output equation, transition table and state table. Also draw a state diagram.  Fig.Q10(b)	**12**	**L4**	**CO6**

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